STD38NH02L

N-CHANNEL 24V - 0.011 Ω - 38A DPAK/IPAK STripFET™ III POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD38NH02L	24 V	< 0.0135 Ω	38 A

- TYPICAL R_{DS}(on) = 0.011 Ω @ 10 V
- TYPICAL R_{DS}(on) = 0.015 Ω @ 5 V
- $R_{DS(ON)}$ * Qg INDUSTRY's BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- THROUGH-HOLE IPAK (TO-251) POWER PACKAGE IN TUBE (SUFFIX "-1")
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")

IPAK
TO-251
(Suffix "-1")

DPAK
TO-252
(Suffix "T4")
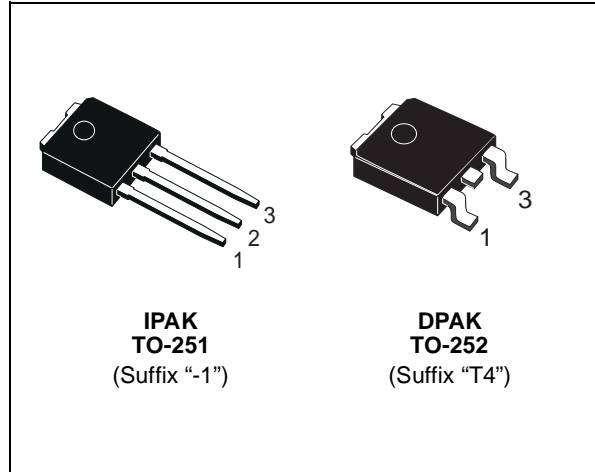
DESCRIPTION
The STD38NH02L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable fot the most demanding DC-DC converter application where high efficiency is to be achieved.

APPLICATIONS
- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTES

INTERNAL SCHEMATIC DIAGRAM

SC08440
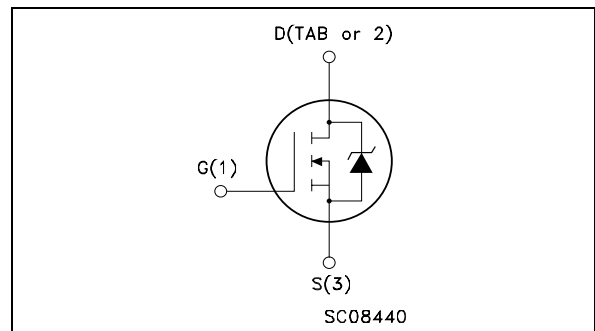
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{spike(1)}$	Drain-source Voltage Rating	30	V
V_{DS}	Drain-source Voltage (V_{GS} = 0)	24	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	24	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C	38	A
I_D	Drain Current (continuous) at T_C = 100°C	27	A
I_{DM}[2]	Drain Current (pulsed)	152	A
P_{tot}	Total Dissipation at T_C = 25°C	40	W
	Derating Factor	0.27	W/°C
E_{AS} [3]	Single Pulse Avalanche Energy	250	mJ
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Max. Operating Junction Temperature		

STD38NH02L

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	3.75	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	100	°C/W
T$_l$	Maximum Lead Temperature For Soldering Purpose		275	°C

ELECTRICAL CHARACTERISTICS (T$_{CASE}$ = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V$_{(BR)DSS}$	Drain-source Breakdown Voltage	I$_D$ = 25 mA, V$_{GS}$ = 0	24			V
I$_{DSS}$	Zero Gate Voltage Drain Current (V$_{GS}$ = 0)	V$_{DS}$ = 20 V V$_{DS}$ = 20 V T$_C$ = 125°C			1 10	µA µA
I$_{GSS}$	Gate-body Leakage Current (V$_{DS}$ = 0)	V$_{GS}$ = ± 20V			±100	nA

ON (4)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$ = V$_{GS}$ I$_D$ = 250 µA	1	1.8		V
R$_{DS(on)}$	Static Drain-source On Resistance	V$_{GS}$ = 10 V I$_D$ = 19 A V$_{GS}$ = 5 V I$_D$ = 9.5 A		0.011 0.015	0.0135 0.025	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g$_{fs}$ (4)	Forward Transconductance	V$_{DS}$ = 10 V I$_D$ = 19 A		19		S
C$_{iss}$ C$_{oss}$ C$_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V$_{DS}$ = 15V f = 1 MHz V$_{GS}$ = 0		1070 305 45		pF pF pF
R$_G$	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		1		Ω

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 10$ V $\quad$ $I_D = 19$ A $R_G = 4.7$ Ω $\quad$ $V_{GS} = 10$ V (Resistive Load, Figure 3)		7 62		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	0.44V $\leq V_{DD} \leq 10$V, $\quad$ $I_D = 38$ A $V_{GS} = 10$ V		18 4 2.5	24	nC nC nC
Q_{oss}(5)	Output Charge	$V_{DS} = 16$ V $\quad$ $V_{GS} = 0$ V		6.5		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 10$ V $\quad$ $I_D = 19$ A $R_G = 4.7\Omega$, $\quad$ $V_{GS} = 10$ V (Resistive Load, Figure 3)		25 12	16	ns ns

SOURCE DRAIN DIODE

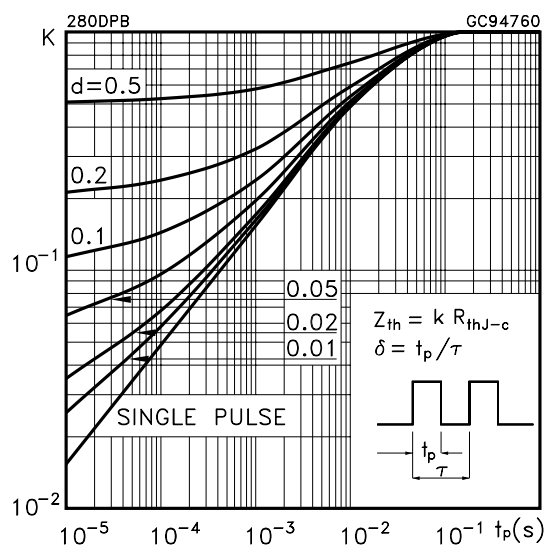| Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				38 152	A A
V_{SD} (4)	Forward On Voltage	$I_{SD} = 19$ A $\quad$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 38$ A $\quad$ $di/dt = 100$A/μs $V_{DD} = 18$ V $\quad$ $T_j = 150°$C (see test circuit, Figure 5)		27 22 1.6		ns nC A

(1) Garanted when external Rg=4.7 Ω and $t_f < t_{fmax}$.
(2) Pulse width limited by safe operating area
(3) Starting T_j = 25 ^{o}C, I_D = 19A, V_{DD} = 18V .

(4) Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
(5) $Q_{oss} = C_{oss}*\Delta V_{in}$, $C_{oss} = C_{gd} + C_{ds}$. See Appendix A
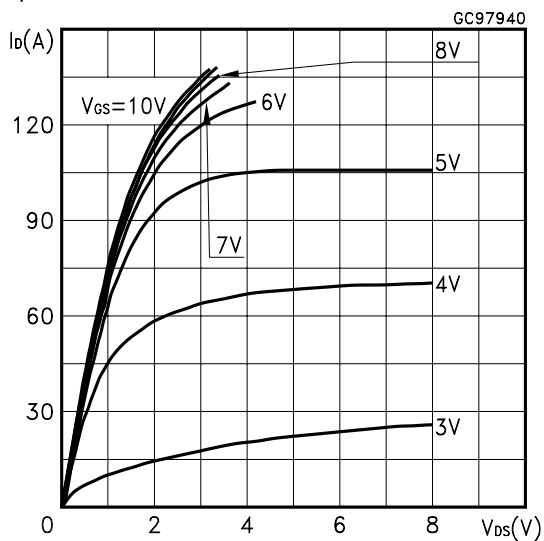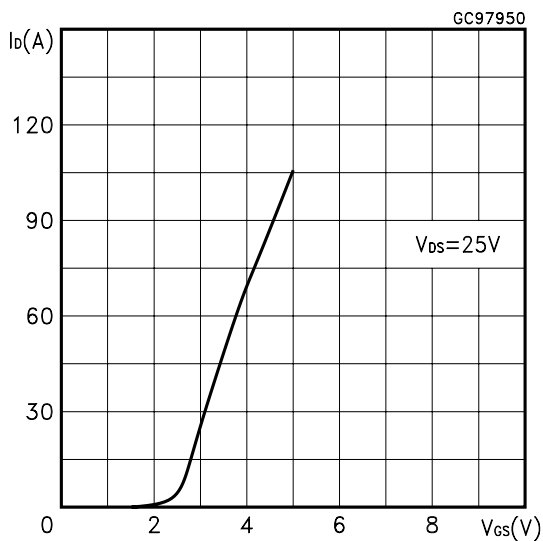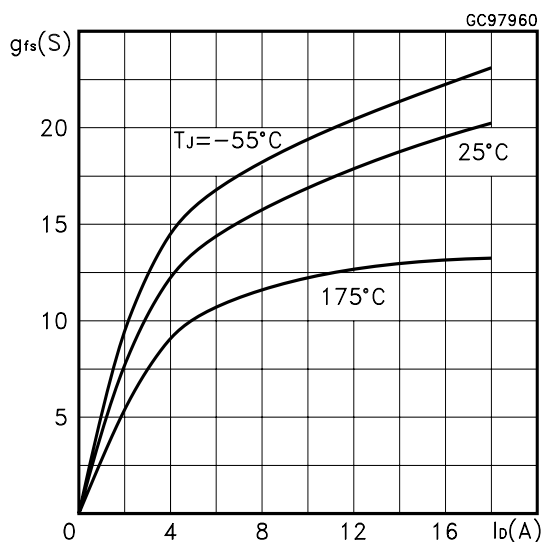
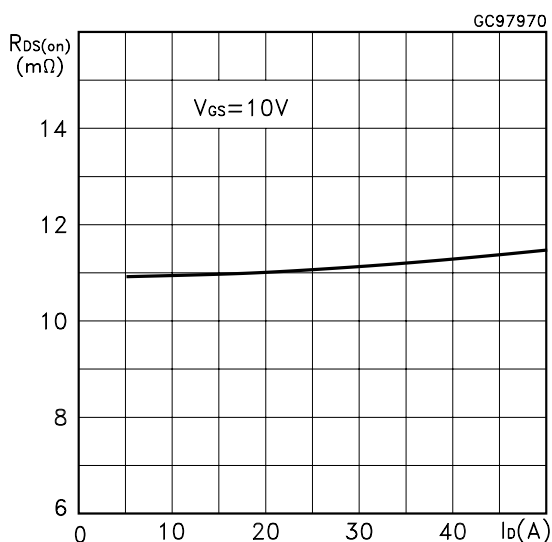Safe Operating Area
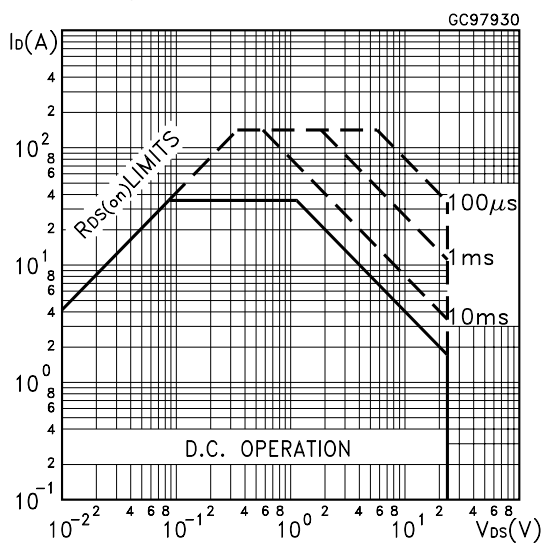
Thermal Impedance

STD38NH02L

Output Characteristics

GC97940

ID(A)

8V

VGS=10V — 6V

120

5V

90

7V

60

4V

30

3V

0   2   4   6   8   VDS(V)

Transfer Characteristics

GC97950

ID(A)

120

90

VDS=25V

60

30

0   2   4   6   8   VGS(V)

Transconductance

GC97960

gfs(S)

20   TJ=−55°C

25°C

15

175°C

10

5

0   4   8   12   16   ID(A)

Static Drain-source On Resistance

GC97970

RDS(on) (mΩ)

VGS=10V

14

12

10

8

6

0   10   20   30   40   ID(A)

Gate Charge vs Gate-source Voltage

GC97980

VGS(V)

VDS=10V
ID=38A

8

6

4

2

0   4   8   12   16   Qg(nC)
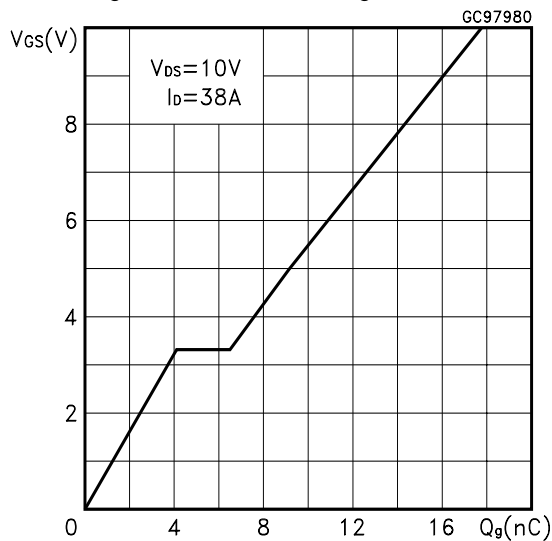
Capacitance Variations

GC97990

C(pF)

f=1MHz
VGS=0V

1600

1200   Ciss

800

400   Coss

Crss

0   3   6   9   12   VDS(V)
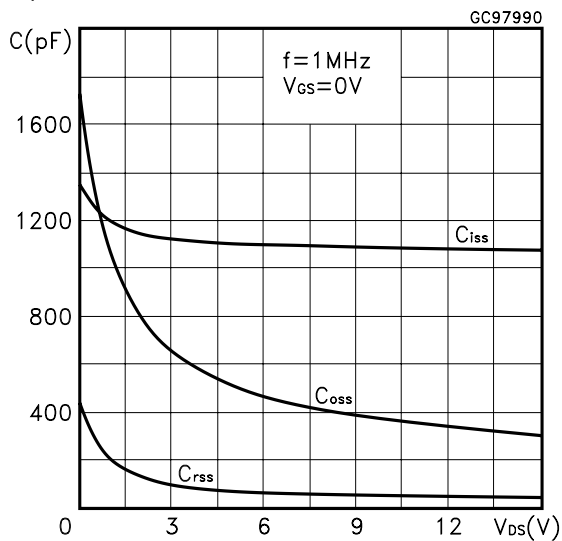
STD38NH02L

Normalized Gate Threshold Voltage vs Temperature

```
VGS(th)
(norm)
                          GC98000

1.0                 VDS=VGS
                    ID=250µA
0.8

0.6

0.4

0.2
      -50    0    50   100   TJ(°C)
```
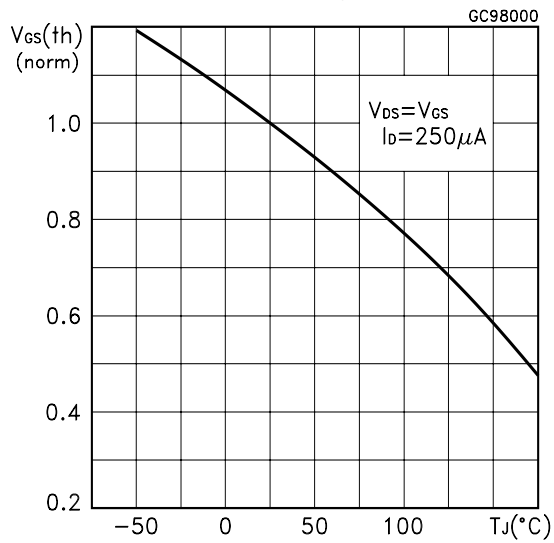
Normalized on Resistance vs Temperature

```
RDS(on)
(norm)           VGS=10V
                          GC98010
                 ID=19A
1.8

1.4

1.0

0.6

0.2
      -50    0    50   100   TJ(°C)
```
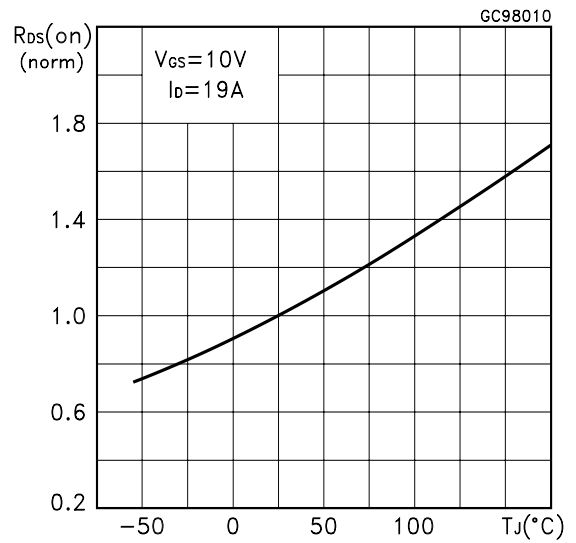
Source-drain Diode Forward Characteristics

```
VSD(V)
                          GC98020

1.6

      TJ=-55°C
1.2                    25°C

0.8
              175°C

0.4

   0   10   20   30   40  ISD(A)
```
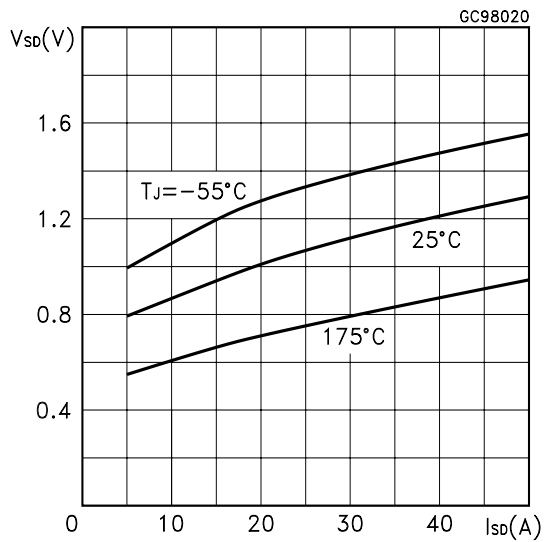
Normalized Breakdown Voltage vs Temperature

```
V(BR)DSS
(norm)       VGS=0
                          GC98030
             ID=250µA
1.1

1.05

1.0

0.95

0.9
      -50    0    50   100   TJ(°C)
```
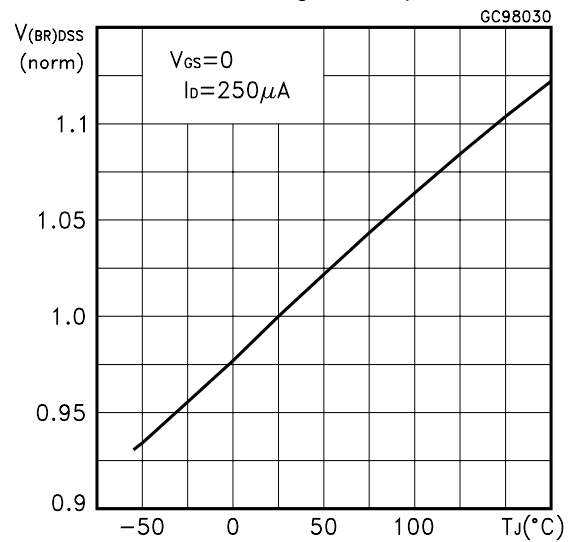
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![ST logo]

Fig. 1: Unclamped Inductive Load Test Circuit

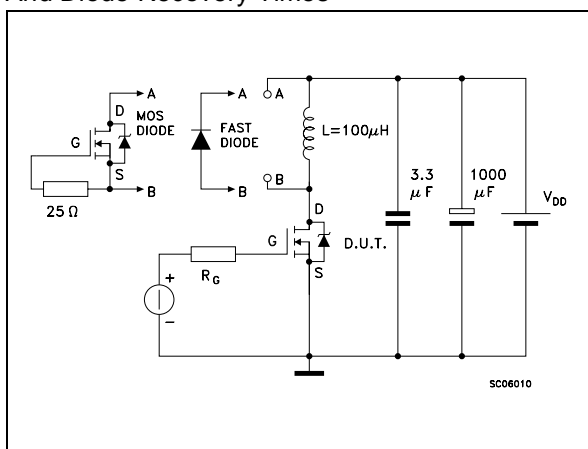**Fig. 2:** Unclamped Inductive Waveform

Fig. 3: Switching Times Test Circuits For Resistive Load


Fig. 4: Gate Charge test Circuit

Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

0068771-E
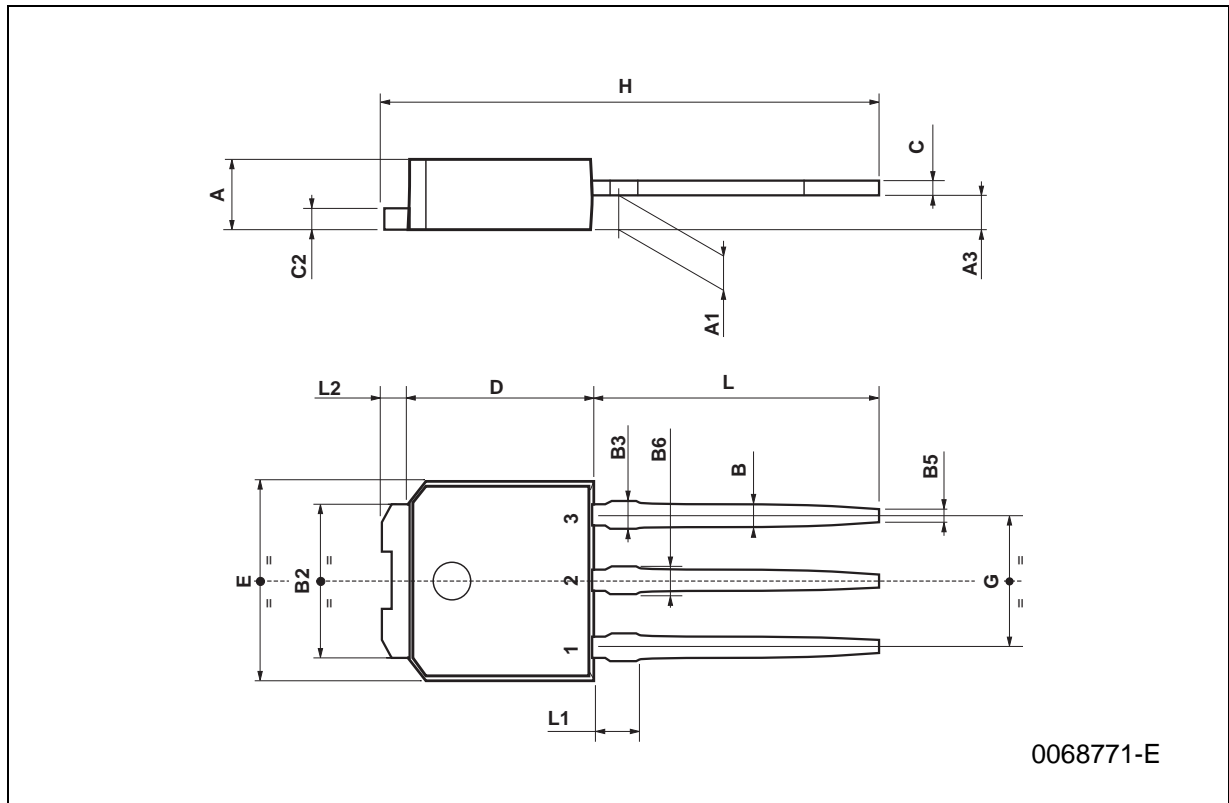
TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039

DETAIL "A"

DETAIL "A"

0068772-B

DPAK FOOTPRINT

6.7 1.8 3.0 1.6

6.7

2.3

2.3

1.6

All dimensions are in millimeters

TUBE SHIPMENT (no suffix)*

0.6 (±0.1)

21.3 (±0.2)

6 (±0.1)

BASE QTY
75

BULK QTY
3000

Tube length 532 (±0.5)

All dimensions are in millimeters
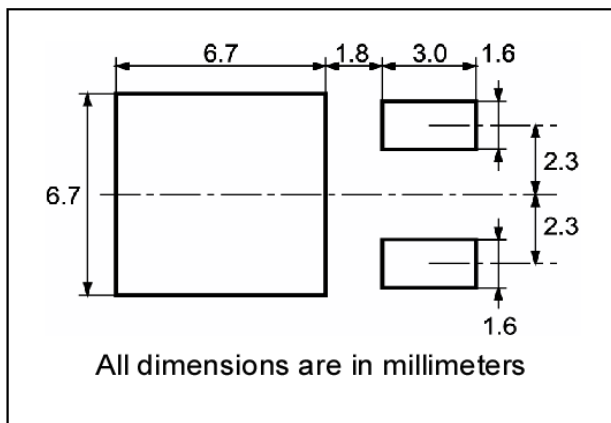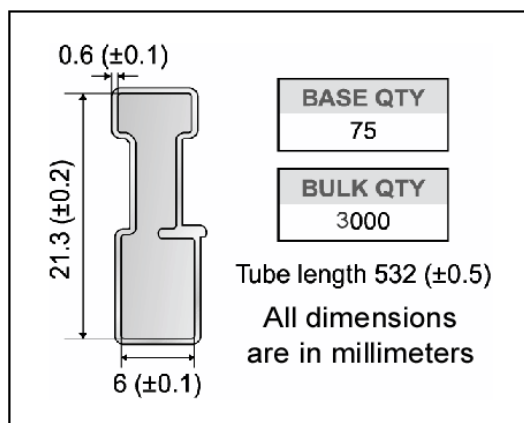
TAPE AND REEL SHIPMENT (suffix "T4")*

40 mm min.
Access hole
at slot location

Full radius

Tape slot
in core for
tape start
2.5mm min.
width

G measured
at hub

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

10 pitches cumulative
tolerance on tape
+ / − 0.2 mm

TOP
COVER
TAPE

For machine ref.
only including
draft and radii
concentric
around B0

Center line
of cavity
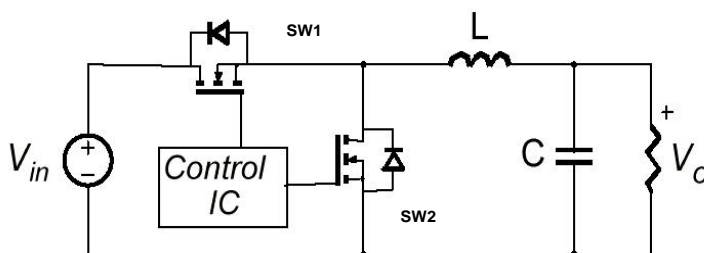
User Direction of Feed

TRL

FEED DIRECTION

R min.

Bending radius

APPENDIX A
Buck Converter: Power Losses Estimation

The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (**SW2**) device requires:

- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Q_{gls} to reduce the gate charge losses
- Small C_{oss} to reduce losses due to output capacitance
- Small Q_{rr} to reduce losses on SW_1 during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;

The high side (**SW1**) device requires:
- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses.

		High Side Switch (SW1)	Low Side Switch (SW2)
$P_{conduction}$		$R_{DS(on)SW1} * I_L^2 * d$	$R_{DS(on)SW2} * I_L^2 * (1-d)$
$P_{switching}$		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \dfrac{I_L}{I_g}$	Zero Voltage Switching
P_{diode}	Recovery	Not Applicable	$^1 V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not Applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
$P_{gate(Q_G)}$		$Q_{g(SW1)} * V_{gg} * f$	$\mathbf{Q_{gls(SW2)} * V_{gg} * f}$
P_{Qoss}		$\dfrac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\dfrac{V_{in} * Q_{oss(SW2)} * f}{2}$

Parameter	Meaning
d	Duty-cycle
Q_{gsth}	Post threshold gate charge
Q_{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
P_{Qoss}	Output capacitance losses

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[1] Dissipated by SW1 during turn-on